**FLIP-FLOPS AND SEQUENTIAL CIRCUITS**

**Latches**

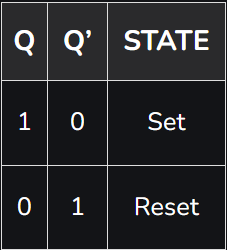
* Stores **single bit** of information.
* Works as **temporary** storage until updated.
* Level sensitive device.

**Types of Latches**

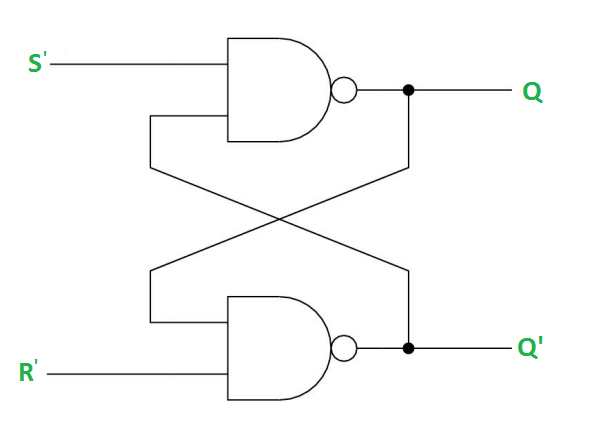
* **SR (set reset) latches:-**
  + Also called present and clear state.
  + Implemented using 2 inputs (set and reset).
  + S sets output to 1.
  + R resets output to 0.
  + Both S and R as 1 means undefined.
  + 2 outputs: Q, Q’
* **D (data) latches:-**
  + Also called transparent latches.
  + Implemented using D and clock signal.
  + If clock is HIGH, then output is carried as per D.
  + If LOW, then it waits for next clock pulse.

**Latches Applications**

* Data storage
* Control circuits
* Flip-flop circuits
* Sequential circuits



* **D-latch using NAND gates:**

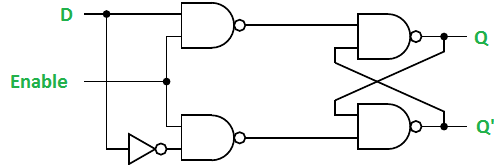


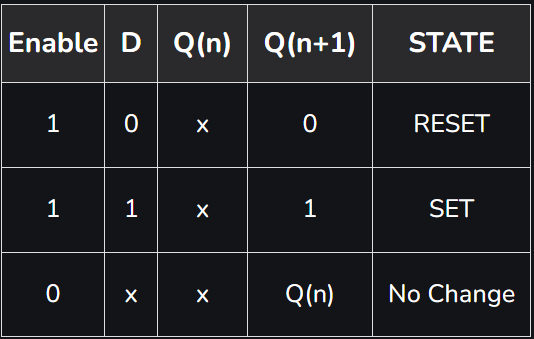
* Can also be implemented using **XNOR** gates
* **Q** is called **reset state**.

**Possible Cases of Latch**

* **Case 1:** S’=R’=1 (S=R=0)
* **Case 2:** S’=0, R’=1 (S=1, R=0)
* **Case 3:** S’=1, R’=0 (S=0, R=1)
* **Case 4:** S’=R’=0 (S=R=1)

**D-latch With Enable**



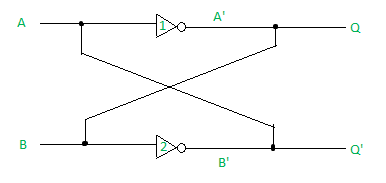


**Merits & Demerits of Latches**

1. **Advantages:-**
   1. Easy implementation
   2. Low power consumption
   3. High speed
   4. Low cost
   5. Versatility (variety of uses)
2. **Disadvantages:-**
   1. No clock (unpredictable behaviour)
   2. Unstable state
   3. Complex timing (no real time applications)

**1-bit Memory Cell**

* Also called **basic bistable element**.
* Stores **1-bit** information temporarily.
* Building block of latches, flip-flops and state machines.
* **Types of 1-bit memory cells:-**
  + SR flip-flops
  + D flip-flops
* Applications are same as latches.
* It is called **bistable** as the circuit is stable unlike latches.



* Imagine its all possible cases yourself.
* The circuit has two stable states: set state (Q=1) & reset state (Q=0)
* Latched means “locked”.
* 1-bit memory cell latches one bit of information.

**Memory Devices**

* **SRAM:**
  + Static random access memory.
  + Fast switching speed.
  + Needs constant power supply, being volatile.
  + Memristors: Reducing electricity supply.
* **Memristors:**
  + SRAM, RAM and flash drives are nowadays replaced by memristors.
  + Can maintain resistive switch despite having no power supply (up to 10 years).
  + Fast switching speed.
  + Low energy consumption.
  + Non-volatile.
  + Small device size.
  + Great endurance and scalability.
* **NAND based flash drives:**
  + No retention ability.
  + Fast switching speed.
  + Low scalability.

**Merits & Demerits of 1-bit Memory Cells**

1. **Advantages:-**
   1. Simple circuit
   2. Cheap setup
   3. Flexibility
   4. Speed
   5. Low power consumption
2. **Disadvantages:-**
   1. Complex circuit
   2. Limited storage
   3. Expensive setup

**Application of 1-bit Memory Cell**

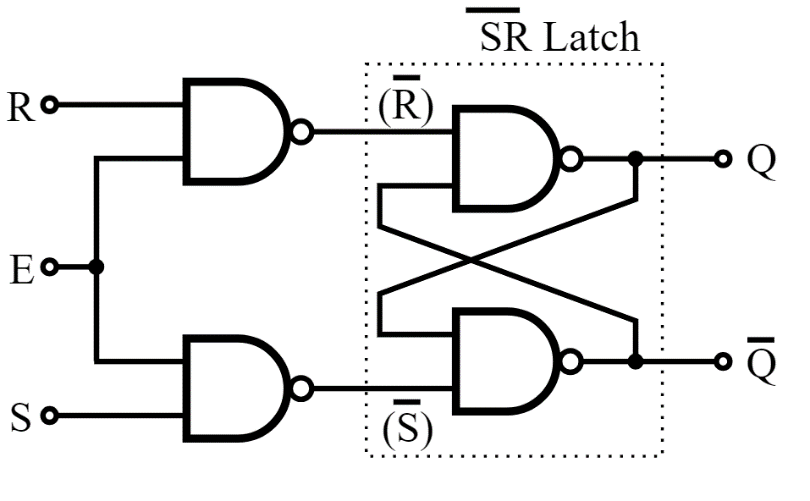
* Registers (stores double, used in processors & chips)
* Flip-flops
* Clock circuits (for storing clock signals)
* Counters (counts clock cycles)

**Flip-Flops**

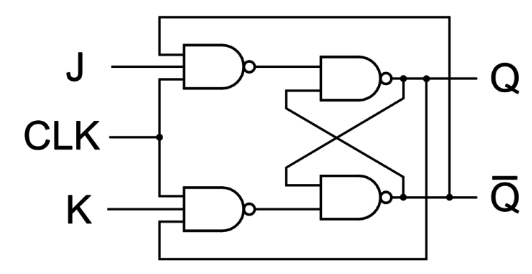
* Input based state changing device.
* **Construction:** 4 NAND gates, 4 NOR gates.
* Also known as **basic digital memory circuit**, **bistable multivariable**.
* Has two outputs of opposite state.

**Types of Flip-Flops**

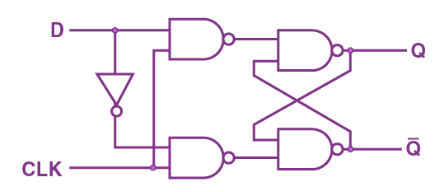
* **SR flip-flop:**
  + State of circuit keeps changing.
  + Must be initialized in set or reset form in starting.
  + Initialization is done by **PR (present)** and **CLR (clear).**



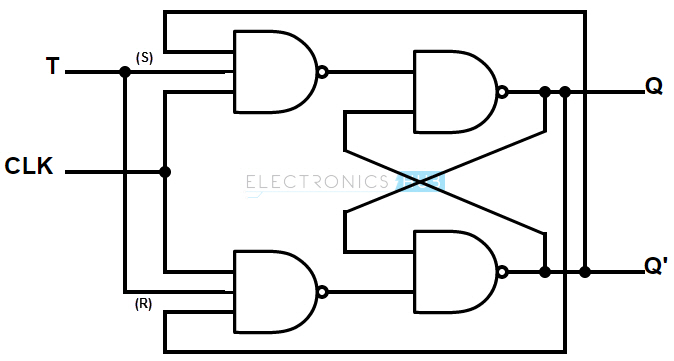
* + **Cases:-**
    - PR=CLR=1 (when Q=Q’=0) normal response to CLK
    - PR=0, CLR=1 (when Q=1)
    - PR=1, CLR=0 (when Q’=1)
    - PR=CLR=0 (invalid state)
* **JK flip-flop:**



* + Cases are same as SR.
  + **Toggle:** Change of Q=0, Q’=1 to Q=1, Q’=0.
  + **Race around condition:** At Q=Q’=1 the input is HIGH for little longer and continuous toggle happens there (main reason is **clk=1**).
* **D flip-flop:**



* **T flip-flop:**

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**Characteristic Equations for Flip-Flops**

* **SR flip-flop**

**QN+1 = QNR’ + SR’**

* **JK flip-flop**

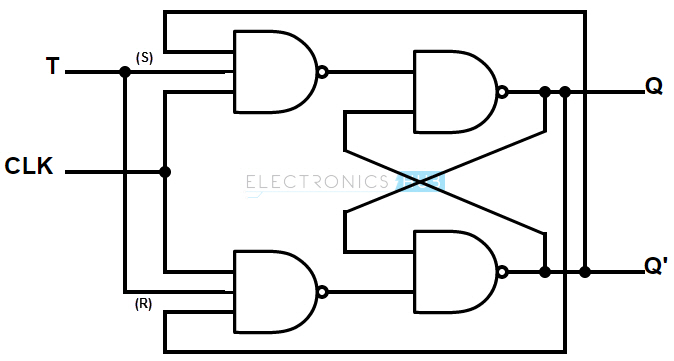
**QN+1 = JQ’N + K’QN**

* **D flip-flop**

**QN+1 = D**

* **T flip-flop**

**QN+1 = QN XOR T**

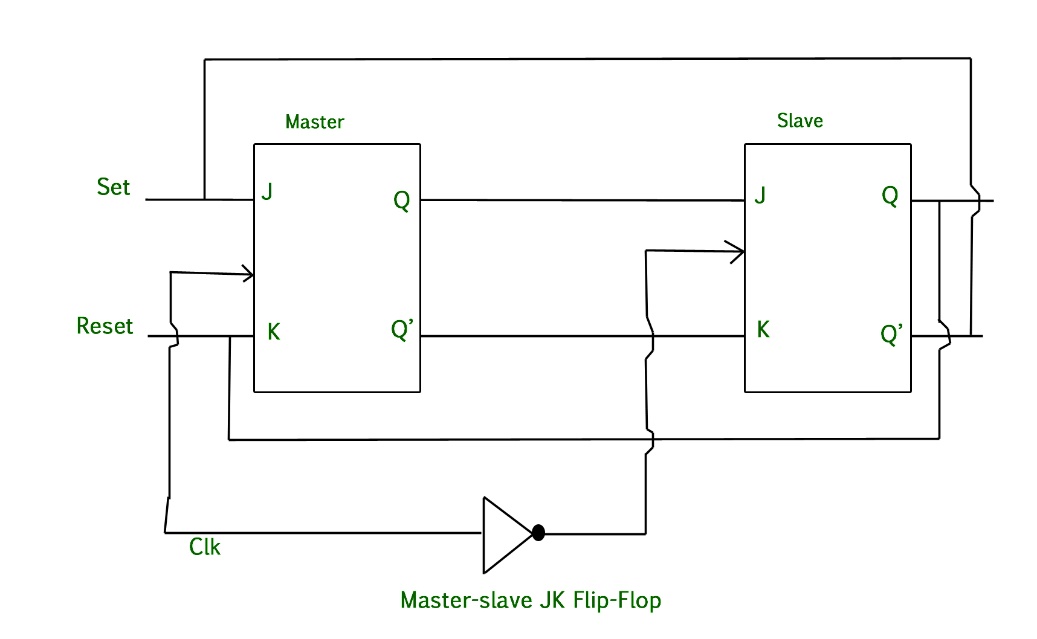


**Application of Flip-Flops**

* Counters
* Frequency dividers
* Shift registers (series of flip-flops)
* Storage registers
* Latch

**Master Slave JK Flip-Flop**

* Race around condition can be avoided by keeping **clk=1** for **short** duration of time.
* **Master slave JK flip-flop** is used for addressing this issue.
* Two JK flip-flop connected in series.

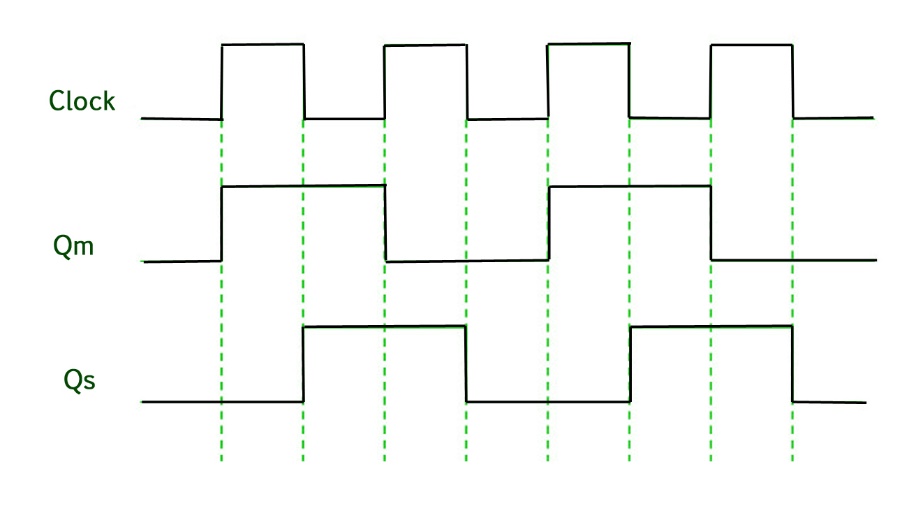


* The thing between J and K **is** **clock**.
* When master’s CP=0, slave’s CP=1 and vice versa.
* **CP:** Clock pulse

**Working of Master Slave JK Flip-Flop**

**\*Write all cases when asked.**

**Timing Diagram of Master Slave Flip-Flop**



**\*Write all possible bullsh\*t about figure above when asked about timing of MSFF**

* It is **synchronous** as it passes data as per clock signals.

Introduction to Sequential Circuits

* Unlike combinational circuits, remembers and uses previously stored memory.
* Used in making timers, clocks, memory elements.
* Implemented using flip-flops.

Types of Sequential Circuits

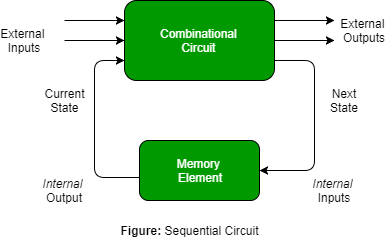
* Finite state machine (FSM)
  + Limited states.

State machine: Mathematical logic model used for storing data.

* + Used in state machines and control systems.
* Synchronous sequential circuits (SSC)
  + Infinite states.
  + Used in timers, counters and memory.

Sequential Circuit

* Output is based on current and previous, input and output.
* Its elements store multiple binary bits of information.
* Basically, a latch in it storing one bit of information.



* External inputs are not controlled by the circuit.
* Internal inputs are from previous output state.